Patent claims

1. A semiconductor circuit arrangement (76), having a substrate (10), which carries in the order specified:
a doped semiconductor layer (14) of a first conductivity type,
an electrically insulating layer (16),
and an electrically conductive or an electrically insulating charge-storing layer (18), which is suitable for the storage of charges,
and having at least one trench (32), which penetrates through the charge-storing layer (18) and also extends into the doped semiconductor layer (14),
the trench (32) penetrating through the doped semiconductor layer (14).

2. The circuit arrangement (76) as claimed in claim 1, featuring a plurality of trenches arranged next to one another, between which in each case a multiplicity of memory cells are arranged, in particular EEPROM memory cells or flash EEPROM memory cells,
and/or the charge-storing layer (18) being subdivided into charge-storing regions transversely with respect to the direction in which the trenches (40) run.

3. The circuit arrangement (76) as claimed in claim 1 or 2, featuring a doped semiconductor layer (12) arranged between the doped semiconductor layer (14) and the substrate (10) and having a conduction type opposite to the first conduction type,
the trench (32) also penetrating through the semiconductor layer (12) of opposite conduction type and extending into the substrate (10),

or the trench (32) ending in the semiconductor layer (12) of opposite conduction type.

4. The circuit arrangement (76) as claimed in one of the preceding claims, featuring an electrically conductive layer (72) and a further electrically insulating layer (70) arranged between the electrically conductive layer (72) and the charge-storing layer (18).

5. The circuit arrangement (76) as claimed in one of the preceding claims, featuring at least one trench (100), which is shallower and wider in comparison with the trench (32) penetrating through the electrically insulating layer (16) and which is arranged in the semiconductor layer (14) of the first conductivity type and through which penetrates the deep trench (32) penetrating through the charge-storing layer (18).

6. The circuit arrangement (76) as claimed in claim 5, wherein the shallow trench (100) does not penetrate through the charge-storing layer (18) and/or the electrically insulating layer (16),
and/or wherein the shallow trench (100) is filled with an electrically insulating material or contains an electrically insulating material, preferably polycrystalline silicon,
and/or wherein the shallow trench (100) projects (A) symmetrically beyond the deep trench (32).

7. The circuit arrangement (76) as claimed in one of the preceding claims, featuring at least one further shallow trench through which no trench penetrates,
and/or the shallow trench (100) through which the deep trench (32) penetrates being arranged in a memory cell array and the shallow trench through

which a trench does not penetrate being arranged in a logic circuit arrangement,
and/or at least one shallow trench (100) through which a deep trench (32) penetrates having the same depth as at least one shallow trench through which a deep trench does not penetrate.

8. The circuit arrangement (76) as claimed in claim 4 and as claimed in one of claims 5 to 7, wherein the electrically conductive layer (72) and/or the further electrically insulating layer (70) extend(s) at least partly into the shallow trench (100).

9. The circuit arrangement (76) as claimed in one of the preceding claims, featuring a further charge-storing layer (110), which adjoins the charge-storing layer (18) through which the trench (32) penetrates,
and at least one cutout (120) arranged in the further charge-storing layer (110), the bottom of which cutout preferably lies completely within the edge of the deep trench (32) and/or the shallow trench (100),
the trench (32) preferably not penetrating through the further charge-storing layer (110).

10. The circuit arrangement (76) as claimed in one of the preceding claims, wherein the trench (32) is filled with an electrically insulating material or contains an electrically insulating material, in particular an oxide, preferably silicon dioxide,
and/or wherein the trench (32) contains an electrically conductive or electrically semiconducting material insulated from the trench wall, in particular a polycrystalline material, preferably polycrystalline silicon, which is doped or undoped.

11. A method for fabricating a semiconductor circuit arrangement (76), in particular a circuit arrangement (76) as claimed in one of the preceding claims,
having the following steps which are formed with no restriction by the order specified:
production of a doping of a first conductivity type in a semiconductor layer (14),
application of an electrically insulating layer (16) before or after the production of the doping,
application of an electrically conductive or of a further electrically insulating charge-storing layer (18), which is suitable for the storage of charge, after the application of the electrically insulating layer (16),
introduction of a trench (32), which penetrates through the electrically insulating layer (16) and the charge-storing layer (18) and which penetrates through the semiconductor layer (14) in a thickness which is greater than the thickness of the doped semiconductor layer (14).

12. The method as claimed in claim 11, featuring the following steps:
application of a mask layer (20), in particular of a photoresist layer or of a hard mask layer, after the application of the charge-storing layer (18),
introduction of the trench (32) with the aid of the mask layer (20).

13. The method as claimed in claim 12, featuring the following steps:
removal of the mask layer (20) after the introduction of the trench (32),
filling of the trench (32) with a filling material (42) after the removal of the mask layer (20),
etching-back of the filling material (42),
or the following steps:

filling of the trench (32) with a filling material (42a) with the mask layer (20a) still present, and etching-back of the filling material (42a) with the mask layer (20a) still present.

14. The method as claimed in one of claims 11 to 13, featuring the following steps:
production of an edge layer (40) at the edges of the trench (32), preferably by thermal oxidation, before the filling of the trench (32) with a filling material (42).

15. The method as claimed in claim 13 or 14, wherein the filling material (42) is etched back to an extent such that a region uncovered during the etching-back process also extends into a region in which the semiconductor layer (14) was originally arranged,
and/or filling of the uncovered region with a further filling material (50), preferably with an oxide.

16. The method as claimed in one of claims 11 to 15, featuring the following steps:
introduction of at least one trench (100), which is shallower and wider in comparison with the trench (32b), into the semiconductor layer (14b) before the application of the charge-storing layer (18b),
filling of the shallow trench (100) before the application of the charge-storing layer (18b),
planarization of the trench filling of the shallow trench (100) before the application of the charge-storing layer (18b).

17. The method as claimed in claim 16, wherein at least one shallow trench (100) is arranged in a region through which a deep trench (32b) later penetrates,

a deep trench (32) preferably not penetrating through at least one shallow trench.

18. The method as claimed in claim 15 and claim 16 or 17, wherein the further filling material (50b) is etched back to an extent such that a region (60b) uncovered during the etching-back process also extends into a region in which the semiconductor layer (14b) was originally arranged,
and/or filling of the uncovered region (60b) with a further electrically insulating layer (70b) and/or with an electrically conductive layer (72b).

19. The method as claimed in one of claims 11 to 18, featuring the following steps:
application of at least one further electrically conductive or electrically insulating charge-storing layer (110) adjoining the other charge-storing layer (18) after the introduction and filling of the trench (32c),
patterning of the further charge-storing layer, preferably before the application of further layers.

20. The method as claimed in claim 19, wherein a cutout (120) arising during the patterning of the further charge-storing layer (110) is extended right into the trench (32c).